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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,651	04/18/2001	Robert Warren Sherburne, Jr		9125

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EXAMINER	
BUTLER, DENNIS	
ART UNIT	**PAPER NUMBER**
2115	7

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,651	SHERBURNE, JR, ROBERT WARREN	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on April 18, 2001. Claims 1-20 are pending.

2. Applicant is advised that should claim 15 be found allowable, claim 18 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the claim is unclear as to the relationship between the one or more processing units each having a clock input and the plurality of clock outputs each coupled to the clock inputs because the claim language calls for one processing unit having one clock input while the controller is recited as having a plurality of clock outputs each coupled to clock inputs. It is unclear whether there can be a plurality of clock outputs each coupled to clock inputs when the claim calls for only one clock input.

Claims 1-20 are rejected because they incorporate the deficiencies of claim 1.

Regarding claims 5 and 11, the relationship between the clocking recited in claim 5, the algorithm recited in claim 11 and the clocking frequency to optimize power consumption and processing power recited in claim 1 is unclear. It is unclear whether reducing peak power dissipation or reducing the average power dissipation or minimizing buffer memory size or emissions control optimizes power consumption and processing power as required by claim 1.

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-3, 6, 9 and 19-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 and 6 of copending Application No. 09/814,355. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention including one or more processing units and a controller varying the clock frequency to each processing unit. Although claims 1-3 and 6 of the present application do not recite the processor including a memory, it is well known that

processors routinely include memory units. In addition, claims 19 and 20 of the present application recite the processor including a buffer memory.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3-6, 9-12, 14-15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiyama et al., U. S. Patent 5,790,877.

Per claim 1:

A) Nishiyama et al teach the following claimed items:

1. one or more processing units each having a clock input that controls the performance of the unit with elements 103, 104 and 105 figure 1, at column 2, lines 37-41 and at column 3, lines 43-49;

2. a controller having a plurality of clock outputs each coupled to the clock inputs with CLK CONT 101 of figure 1 and at column 3, lines 43-60;

3. the controller varying the clock frequency of each processing unit to optimize power consumption and processing power for a task at column 2, lines 51-65, at column 3, lines 50-67 and at column 6, lines 8-17.

Per claims 3-6, 9-12, 14-15 and 18:

Nishiyama describes one of the processing unit comprises a RISC processor at column 3, lines 35-42. Nishiyama describes dynamically managing each unit on a per task basis at column 2, lines 37-65 and at column 6, lines 9-18. Nishiyama describes each unit clocked at the lowest rate possible to reduce peak power dissipation or average dissipation at column 2, lines 52-60 and at column 6, lines 9-18. Nishiyama describes the controller generating a plurality of clock signals with figure 2 and independently controlling the rate to each processing unit at column 3, lines 64-67 and at column 4, lines 21-34. Nishiyama describes the clock rate based on a pre-assigned algorithm optimized for power reduction with the compiler, figures 5 and 6 and at column 4, line 60 – column 5, line 16. Nishiyama describes controlling clock inputs on-the-fly and a centralized controller at column 3, lines 43-67.

10. Claims 2, 7-8, 13, 16-17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama et al., U. S. Patent 5,790,877 in view of Georgiou et al., U. S. Patent 6,047,248.

Per claims 2, 7 and 8:

A) Nishiyama et al teach the items of claims 1 and 6 as described above. The claims seem to differ from Nishiyama et al in that Nishiyama et al fails to

explicitly teach the processing unit comprising a DSP or the plurality of clocks being gated versions of a master clock as claimed. Georgiou teaches that it is known to provide a controller that outputs a plurality of clocks to one or more DSP processing units at column 3, lines 61-65. In addition, Georgiou teaches that it is known to provide gated versions of a master clock with figure 4 and at column 8, lines 37-67. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a controller that outputs a plurality of clocks to one or more DSP processing units or to provide gated versions of a master clock , as taught by Georgiou, in order to apply Nishiyama's power saving system to a processor core having at least one DSP processing unit or to provide the details of implementing Nishiyama's clock generator of figure 2. One of ordinary skill in the art would have been motivated to combine Nishiyama and Georgiou because of Georgiou's suggestion that a clock control system having a plurality of clock outputs coupled to a plurality of functional units can be applied to DSP functional units at column 3, lines 48-65 and because of Nishiyama's suggestion that the clock generator provide a multi-frequency dividable clock for each hardware resource at column 4, lines 31-35. It would have been obvious for one of ordinary skill in the art to combine Nishiyama and Georgiou because they are both directed to the problem of reducing the power consumption of a processor by individually controlling the clock frequency to each processing/functional unit.

Per claims 13, 16-17 and 19-20:

Georgiou describes invoking an algorithm (selecting voltage-frequency pairs) by one or more external system stimuli (thermal sensor input) at column 8, lines 50-67. In addition, Nishiyama describes providing an internal instruction that instructs the clock controller to adjust the frequency for each individual processing unit. Georgiou describes a controller controlling clock inputs in a decentralized manner with the individual thermal sensors (T1-Tk) at each functional unit with figure 1. Georgiou describes generating clock inputs in any arbitrary increments from a master clock with the divide by 2 and the divide by n dividers and associated multiplexers of figure 4 and at column 8, lines 42-67. Georgiou describes a buffer coupled between two processing units with Completion Unit 122 of figure 1 and at column 6, lines 5-7 and 25-29. Georgiou does not explicitly describe using a FIFO buffer. However, FIFO buffers are well known in the art and it would have been obvious to use a FIFO buffer in order to process instructions in a first in first out manner.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler

Dennis M Butler
Primary Examiner
Art Unit 2115